IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	David K. Parker		
Serial No.:	10/814,774	Confirmation No.:	8909
Filed:	March 30, 2004		
For:	DATA STRUCTURES FOR SUPPORTING PACKET DATA MODIFICATION OPERATIONS	Examiner:	Ahmed, Salman
Docket No.:	2717P164	Art Unit:	2476

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY UNDER 37 CFR §1.116 EXPEDITED PROCEDURE

Dear Examiner:

This reply After Final is submitted in response to the Final Office Action mailed April 21, 2010, for the above-noted patent application. Applicants respectfully request the Examiner to please reconsider the claims in section I, beginning on page 2, in view of the remarks in section II, beginning on page 8.

I hereby certify that this correspondence is being deposited via EFS Web on the date below:

June 21, 2010
Date of Deposit

/Merissa R. Anderson/

SECTION I—CLAIMS

Amendment to the Claims:

This listing of the claims will replace all prior versions and listings of claims in the application. Claims 1-3, 6-11, 24, and 29 are amended herein. Claims 4-5, 12-13, 15-17, 19-20, 23, and 25-27 remain canceled herein without prejudice. No new claims are added.

Listing of Claims:

1. (Currently amended) A non-transitory processor readable medium having instructions stored thereon that, when executed by a processor in a switch, cause the switch to perform a method for implementing one or more packet modification operations on a packet received at the switch, wherein the method comprises:

associating a data structure link with the packet received at the switch by inserting a data structure index corresponding to the data structure link into a header of the packet;

retrieving a data structure from memory of the switch via the data structure link associated with the packet, wherein the data structure comprises:

a first pointer to a sequence of commands for execution by a processor of the switch to implement the one or more packet modification operations stored in packed format with more than one command stored in a single addressable entry in a sequence in a first memory area of the memory, and

a second pointer to a burst of data or mask items stored in packed format with more than one data or mask item stored in a single addressable entry in the stored burst in a

second memory area of the memory distinct from the first memory area, the burst of data or mask items for use by the processor in executing the one or more commands;

retrieving the commands in the sequence from the first memory area via the first pointer;

retrieving the data or mask items in the burst from the second memory area via the second pointer; and

performing one or more packet modification operations on the packet by executing the commands in the sequence via the processor using the burst of data or mask items as operands or masks for operands in the one or more packet modification operations performed.

2. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the first and second memory areas are located in different memories.

3. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the first and second memory areas are located in the same memory.

4-5. (Cancelled).

6. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

7. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the first and second memory areas are located in a memory implemented off chip in relation to the processor.

8. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the first memory area is located in a memory implemented on chip in relation to the

processor.

9. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the data structure comprises a plurality of pointers, each to a sequence of commands implementing one or more packet modification operations.

10. (Currently amended) The non-transitory processor readable medium of claim 9 wherein the data structure comprises a plurality of pointers, each to a burst of data or mask items.

11. (Previously presented) A method within a switch for performing one or more packet modification operations on a packet received at the switch, wherein the method comprises:

associating a data structure link with the packet received at the switch by inserting a data structure index corresponding to the data structure link into a header of the packet;

retrieving a data structure from memory of the switch via the data structure link associated with the packet, wherein the data structure comprises:

a first pointer to a sequence of commands for execution by a processor of the switch to implement the one or more packet modification operations stored in packed format with more than one command stored in a single addressable entry in a sequence in a first memory area of the memory, and

a second pointer to a burst of data or mask items stored in packed format with more than one data or mask item stored in a single addressable entry in the stored burst in a second memory area of the memory distinct from the first memory area, the burst of data or mask items for use by the processor in executing the one or more commands;

retrieving the commands in the sequence from the first memory area via the first pointer;

retrieving the data or mask items in the burst from the second memory area via the second pointer; and

performing one or more packet modification operations on the packet by executing the commands in the sequence via the processor using the burst of data or mask items as operands or masks for operands in the one or more packet modification operations performed.

12-13. (Canceled).

14. (Previously presented) The method of claim 11 wherein the first and second memory areas are:

located in different and distinct physical memories;

located in distinct portions of a same physical memory;

located in an internal recipe RAM (Random Access Memory) and an external SRAM (Static Random Access Memory) respectively;

located in a memory implemented off-chip from a modification processor to execute the sequence of commands; or

located in a memory implemented on-chip with the modification processor to execute the sequence of commands.

15-17. (Cancelled).

18. (Previously Presented) The method of claim 11 wherein the data or mask items in the burst comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

19-20. (Cancelled).

21. (Previously presented) The method of claim 11 wherein the data structure comprises a

plurality of pointers, each to a sequence of commands implementing one or more packet modification operations.

22. (Previously presented) The method of claim 11 wherein the data structure comprises a plurality of pointers, each to a burst of data or mask items.

23. (Cancelled).

24. (Currently amended) A packet modification system comprising:

an associator to associate a data structure link with a packet received at the packet modification system by inserting a data structure index corresponding to the data structure link into a header of the packet;

a physical memory to store a data structure comprising:

a first pointer to a sequence of commands implementing one or more packet modification operations and stored in a first memory area of the physical memory in packed format with more than one command stored in a single addressable entry in the stored sequence, and

a second pointer to a burst of data or mask items stored in a second memory area of the physical memory distinct from the first memory area in packed format with more than one data or mask item stored in a single addressable entry in the stored burst; and

a processor to:

retrieve the commands in the sequence from the first memory area via the first pointer;

retrieve the data or mask items in the burst from the second memory area via the second pointer, and

execute the commands in the sequence using the burst of data or mask items as operands

or masks for operands in the one or more packet modification operations.

25-27. (Cancelled).

28. (Previously presented) The system of claim 24 wherein the first and second memory areas are located in different memories.

29. (Currently amended) The system of claim 24 wherein the first and second memory areas are located in the same physical memory.

30. (Previously presented) The system of claim 24 wherein the processor comprises a pipeline processor core to retrieve the commands in the sequence in a first stage, and execute the commands in the sequence in one or more subsequent stages.

SECTION II—REMARKS

Applicants respectfully request reconsideration of the above referenced patent application for the following reasons:

Allowable subject matter

Applicants acknowledge that claims 11, 14, 18, 21 and 22 are allowed.

Claims rejected under 35 U.S.C. § 101

The Office Action rejected claims 1-3, 6-10, 24 and 28-30 under 35 U.S.C. § 101 as being directed toward "non-statutory subject matter."

Claim 1:

With respect to independent claim 1 specifically, the present Office Action states that although claim 1 recites a "processor readable medium," the Office Action nevertheless interprets the claim "as covering both non-statutory subject matter and statutory subject matter" under 35 U.S.C. § 101 asserting that such a claim could be interpreted to "cover[] forms of non-transitory tangible medium **and transitory propagating signals per se** … ."

It appears as though the present rejection is based on improperly reading limitations of the Specification into Applicants' claims, which is contrary to the express guidance set forth under M.P.E.P. § 2111.01(II). For example, the Office Action specifically makes reference to Applicants' specification at page 7 in support of its rejection as disclosing "logic" which the Office Action contends is sufficient to support the above rejection.

The Office Action does however, provide the helpful recommendation that Applicants "avoid a rejection under 35 U.S.C. § 101 by **adding the limitation 'non-transitory' to the claim**." Refer to the present Office Action at page 3, second paragraph.

In the interests of advancing prosecution toward as expeditious of an allowance as feasible, Applicants have introduced the unnecessary, but clarifying limitation, "non-transitory" prior to the term, "processor readable medium," so as to make express that Applicants' claimed embodiment is directed toward patentable subject matter under 35 U.S.C. § 101. Those claims which depend upon independent claim 1 have been amended herein to recite a similar limitation.

Accordingly, Applicants respectfully submit that the amendments to the claims overcome the present rejection and thus, request the Examiner to withdraw the rejection to the claims under 35 U.S.C. §101.

Claim 24:

With respect to independent claim 24, the present Office Action states that although the claim recites a "memory," the Office Action nevertheless contends that a "memory" could be interpreted, again in view of page 7 of Applicants' specification, as an "associator," or a "data structure," or a "pointer," each of which the Office Action contends are "software only, thus making the 'system' claim non-statutory in light of the specification page 7." Refer to the Office Action at page 4, second paragraph.

Again, in the interests of advancing prosecution toward as expeditious of an allowance as feasible, Applicants have introduced the clarifying limitation "physical memory" into independent claim 24.

Such a limitation makes expressly clear that Applicants' claimed embodiment is directed toward patentable subject matter under 35 U.S.C. § 101.

The term "physical memory" is supported by Applicants' specification at, for example, page 7, third paragraph, which teaches:

> The term "**memory**" refers to any **processor-readable *physical* or logical medium**, including but not limited to RAM, ROM, EPROM, PROM, EEPROM, disk, floppy disk, hard disk, CD-ROM, DVD, queue, FIFO or the like, or any combination of two or more of the foregoing, on which may be stored one or more instructions or commands executable by a processor, data, or packets in whole or in part.

Accordingly, Applicants submit that the amendment to the claim overcomes the present rejection. Those claims which depend directly or indirectly upon independent claim 24 incorporate the limitations of independent claim 24, and thus, are directed toward patentable subject matter under 35 U.S.C. § 101 for at least the same reasons.

Accordingly, Applicants respectfully request the Examiner to withdraw the rejection to the claims under 35 U.S.C. §101.

Entry of amendments after Final Rejection:

Applicants respectfully submit that the entry of the above noted clarifying amendments after Final Rejection is appropriate in accordance with M.P.E.P. § 714.13(II) which states that amendments after final may be entered:

> … **where an amendment merely cancels claims, adopts examiner suggestions, removes issues for appeal, or in some other way requires only a cursory review by the examiner**, compliance with the requirement of a showing under 37 CFR 1.116(b)(3) is expected in all amendments after final rejection. … .

More particularly, Applicants respectfully submit that entry of the clarifying limitations "non-transitory" and "physical" represent an adoption of the Examiners' suggestions set forth in the Office Action so as to place the case in immediate condition for allowance and should require "only a cursory review by the examiner," in accordance with M.P.E.P. § 714.13(II) in confirming the allowability of all claims now pending in the application.

CONCLUSION

Given the above remarks, all claims pending in the application are in condition for allowance. If there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (503) 439-8778.

Charge Deposit Account

Please charge our Deposit Account No. 02-2666 for any additional fee(s) that may be due in this matter, and please credit the same deposit account for any overpayment.

Respectfully Submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

/Gregory D. Caldwell/ — June 21, 2010

Gregory D. Caldwell — Date
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